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MIXED SIGNAL LETTER

# Area-efficient multi-channel active matrix micro-LED driver chip design

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**Abstract**
This study develops the control and driver for active Micro LED panel with chip-level design. The chip includes constant current circuit, digital-to-analog converter, SPI control interface, and active-matrix display control. The design process uses TSMC0.18um HVG2 CMOS technology, to realize 30 channels for micro LED driver. To reduce I/O pins, the input signals feed to the dynamic shift register in serial, and the results are loaded to the digital-to-analog converter (DAC) in parallel. The DAC module consists of R2R network, unity-gain buffer and sample-and-hold circuits. The DAC outputs with constant current for micro LED driving from voltage-to-current conversion. To reduce the number of DAC component, one DAC can share the common circuit to drive RGB LED of one pixel based on the selected current mirror structure. This chip can greatly reduce resistor and switches about 92% and 96% respectively, compared with the conventional R DAC structure. The measurements result with good linear for the current dimming control, which the test digital signals are generated by Verilog codes to estimate the gray current of this chip.

**Keywords** Active matrix · Micro LED · Digital-to-analog converter · SPI protocol · Current mode

## 1 Introduction

With the continuous advancement of display technology, the demand for high color depth, high resolution and low cost with active matrix displays is still great requirement. These displays are mainly based on liquid crystal display(LCD) or organic light emitting diodes (OLED). In the circuit of a typical active matrix display, driver IC is an one of the important technique. The driving method can be voltage mode, current mode, or PWM mode. The voltage mode is applied on LCD driving [1–3]. It converts the input digital signal into an analog signal and drives the LCD display panel soon. As for OLED driving, the current mode is employed to keep the linear dimming [4–12]. The extra voltage-to-current converter is required to generate the constant current to drive OLED [13–15]. For Micro-LED driver, one can use current mode [16, 17] or PWM mode [18, 19]. Since micro LED response speed is very fast, it can work on fast PWM signal for gray level control. This is very effective with passive matrix control. However, for active matrix display, each LED requires one PWM generate circuit to keep the brightness in any time. The circuit complexity becomes very high. As the current mode applied on AM micro LED driving, the basic structure likes to that of OLED driving method. Since micro LED is very low power dissipation and high lighting efficiency, its driving current is less than 1 mA in practical applications. Since OLED lighting efficiency is lower than micro LED, the OLED driving current is about 20–50 mA in maximum. Compared with OLED, the driving current for micro LED must be greatly reduced to keep good linear feature. The performance of the driver IC has a crucial impact on the display image quality, because it ultimately determines the brightness of the pixel. In order to meet the demand for high color depth and low cost, the critical flicker fusion frequency of the driver IC should be reduced and the circuit area of the IC should be minimized as possible to save the system area.

For the OLED or micro LED driving method, there are many papers presented with AM or PM matrix. In this study, we interested at active matrix driving due to low flicker in display. An area-efficient 9-bit digital-to-analog converter (DAC) is presented with current-mode active-

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matrix [4], which the DAC is realized with a switched-current architecture, which periodically receives digital bits one by one conversion to high-performance current-mode sample and hold circuit. A fast ramp-voltage-based for current programming is proposed in [7], which uses an external compensation circuit with the second-generation current conveyor and an amplifier. Huang et.at. present external compensation approaches to compensate the different degradation of array pixels to improve linear feature [20], which performs the sensing and compensation synchronously during several continuous display frames. Ahn et.at. attempt to achieve highly uniform luminance using an adaptive reference generator for AMLED display with PWM control [19], which compensates for all resistance mismatches for in one row scanning line by generating respective reference voltages.

In order to reduce the use of switching transistors and resistors, this paper develops R2R method rather than resistor string for the conventional R DAC structure [11], which can greatly reduce the layout area by saving of resistors and switches. In order to share the digital-to-analog converter, the sample-and-hold circuits is proposed on micro LED display to ensure that the driving current of each LED is kept even if the pixel is off-scanning. With this approach, one DAC is repeated to drive RGB pixels with the common circuit to reduce 66% area. The R2R-DAC circuit is well proved by simulation and measurement results using an TSMC 0.18um HVG2 CMOS technology. This paper is organized as follows. The overall architecture of the driver of Micro LED displays is presented in Sect. 2. The chip circuit is described in Sect. 3. The simulation and measurement of the proposed chip are presented in Sect. 4. The conclusions are described in Sect. 5.

## 2 2. System architecture

The overall architecture of the Micro LED display driving circuit is shown in Fig. 1. The chip is designed to drive 10 × 3 micro LEDs per row. Each row-data is sampled and hold for active matrix display. The input data is from the FPGA board that encodes and allocates the dimming data for each pixel with timing slot control, and then the dimming data is sent to the chip with SPI interface. SPI is a serial port that can reduce the chip and FPGA I/O pins and to save package costs. For this, the shift register is used to store the data from SPI with the dynamic circuit. For N pixels driver per row, the 10 N shift registers are designed with serial data transferring in this chip. As for N = 10, after the end of 100 clocks, the current of shift register outputs a row dimming data at this time. The data on shift register is transferred to the R2R DAC for analog voltage output, and then through the voltage to current converter circuit to achieve constant current driver for micro LED. The sample-and-hold circuits that can keep the driving current for micro LED display as they are on off-scanning state. This allows R2R DAC continue to provide to other channels using. The common DAC circuit can be shared for micro LED for various columns. Such that the area can be greatly reduced, and the constant current can also be active to drive micro LED in any time. The active matrix driver can make the micro LED displaying without flicker.

### 2.1 DAC circuit design

The digital dimming code is required to convert to the analog form with DAC circuit. Resistor-string DAC chip is widely used in displaying drivers due to its good linearity between different channels [9, 11]. According to the binary decoder, the series resistors can divide the reference voltage, and then the switch select which one to output. However, the requirement of resistors and switching transistors increase exponentially for high-resolution display. The architecture of the conventional R DAC consists of resistors and switching transistors, which requires $2^{N+1}$ resistors and $2^{N}$ switches for the N-bit conversion, as shown in Fig. 2. Moreover, the binary decoder is required for N-to-$2^{N}$ decoding circuit to control the switch. As using a conventional DAC circuit with 8-bit resolution, the layout area of resistors, switches and routing exceed half of the entire driver chip.

In this design, the R − 2R resistor network is used for digital-to-analog converter, as shown in Fig. 3. The output voltage of digital-to-analog can be obtained from'

$$V_{out} = \sum_{i=0}^{N-1} V_{ref} \times \frac{2^i}{2^N} \tag{1}$$

where N is the number of resolution. The resistance of R and 2R is fixed in a ladder array, which just solves the resistor matching problem in chip process with the ratio of resistance. In fact, it saves more area and has better frequency response capabilities with this approach. The number of control switches is the same as the number of bits, which switches for a part of the signal path to the output with incorporated the R2R circuit resistance. For N-bit conversion, only N-switches and 2N + 1 resistors are required, which can save chip area. Compared with the R DAC structure, the resistors and switches can reduce the

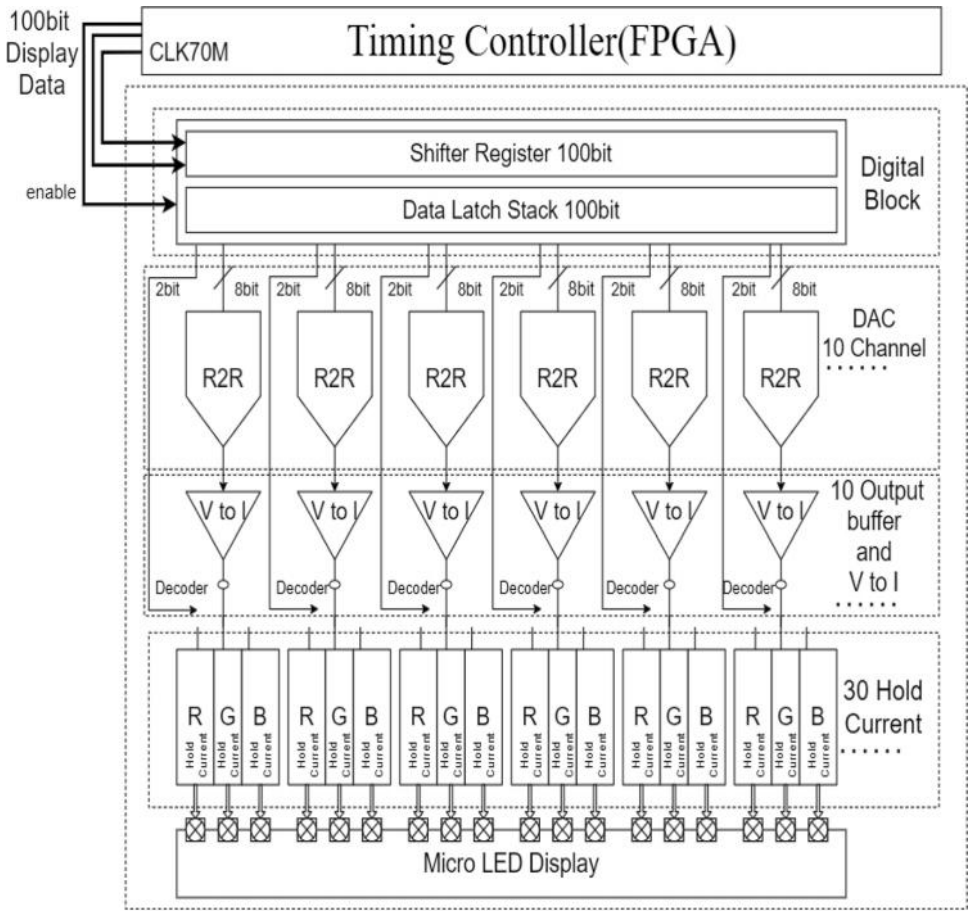



**Fig. 1** The architecture of proposed Micro LED display panel

ratio of $(2^{N+1} - 2\mathrm{N} + 1)/2^{N+1}$ and $(2^N - \mathrm{N})/2^N$ respectively.

## 2.2 AM panel control

Figure 4 shows the sample-and-hold circuit and voltage to current converter to drive AM micro LED pixel. The output of DAC is connected to this circuit. The voltage to current is converted with OPA (operation amplifier). The current can be achieved from

$$I_{D1} = \frac{V_{out}(DAC)}{R_F} \tag{2}$$

Based on the current mirror, the current of Q1 is mirrored to Q2–Q4 by switches S1–S3 control. The RGB LED is driven with the common DAC circuit to save the chip area. The operation is follow. For drive R LED, the S1 is on, S2 and S3 are off. The current of red LED can be given by

$$I_R = \frac{Q_2(W/L)}{Q_1(W/L)} I_{D1} \tag{3}$$

where W and L is channel width and length of MOS respectively. Similarly, when the S2 is on, S1 and S3 are off, one can find the current of green LED from

$$I_G = \frac{Q_3(W/L)}{Q_1(W/L)} I_{D1} \tag{4}$$

When the S3 is on, S1 and S2 are off, the current for blue LED driving can be expressed by

$$I_B = \frac{Q_4(W/L)}{Q_1(W/L)} I_{D1}. \tag{5}$$

For active matrix driving, the LED must be continuously lighting when it is not written a new data. For this function, a sample and hold function is proposed. When S1 turns on, Q2 is to drive red LED. At this time, the current is to charge the capacitor C1 too. If the current is high, the C1 would be charged to the relative voltage. The C1 hold the voltage until the next new data scanning in. Similarly, C2

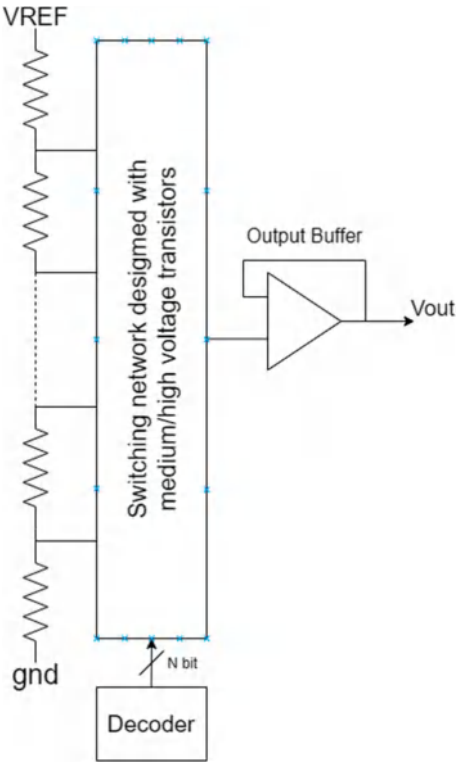



**Fig. 2** The structure of general N-bit R-DAC

and C3 hold the relative voltage to drive green and blue LED. In this chip, we design a current mirror circuit that the current can be copied to the selected output channel with high accuracy. The 2-bit decoder is used to control the switches S1–S3, which select the DAC output to which one channel.

Figure 5 shows the relative of timing diagram of sample and hold circuit for RGB LED. First, the data is written to red LED, and C2 and C3 hold the previous data to keep green and blue LED lighting. Next, the new green data is

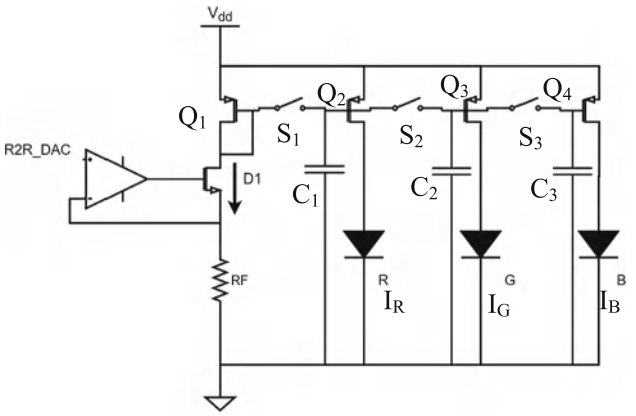



**Fig. 4** The selected current mirror structure for micro LED pixel driving

converted from DAC and V-to-I, to drive green LED and stored the relative voltage to C2. At this time, red and green are continuously lighting with the hold capacitor C1 and C3 respectively. At the next control clock, the digital blue data is written to C3 and drive blue LED with at the same time, while C1 and C2 hold the voltage to drive red and green LED respectively. The DAC output voltage is converted into a current, and the voltage is stored with the capacitance dependent on the selected output channel. During the period of data scanning, the voltage will not be changed until to rewritten. To reduce the flicker, one must keep the hold voltage on the capacitors until the next scanning data in.

## 2.3 Digital control

The dimming data is sent to micro LED with FPGA chip. The SPI format is used for the communication protocol between this chip and FPGA. Figure 6 shows each LED control with address and data. The address is to control

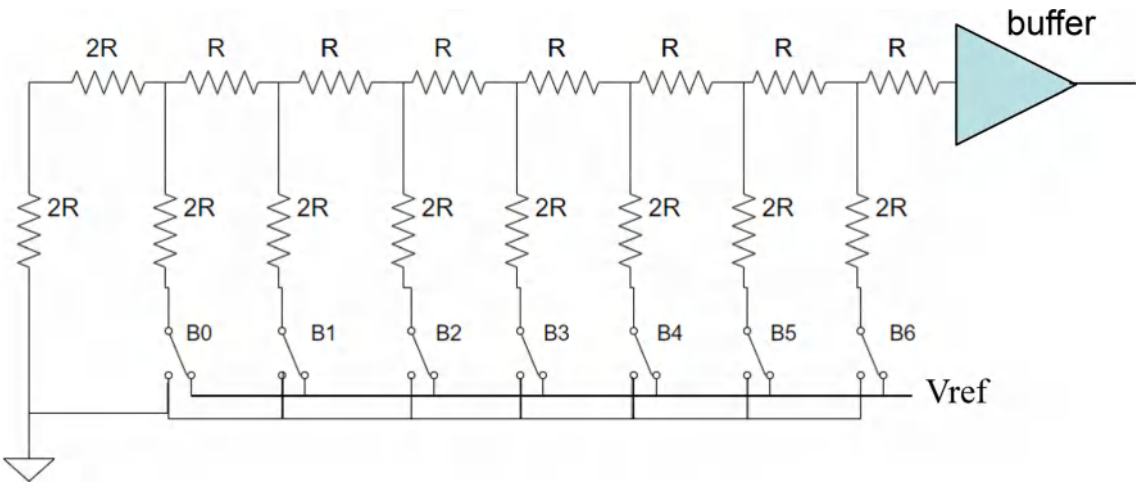



**Fig. 3** The R2R-based digital-to-analog converter

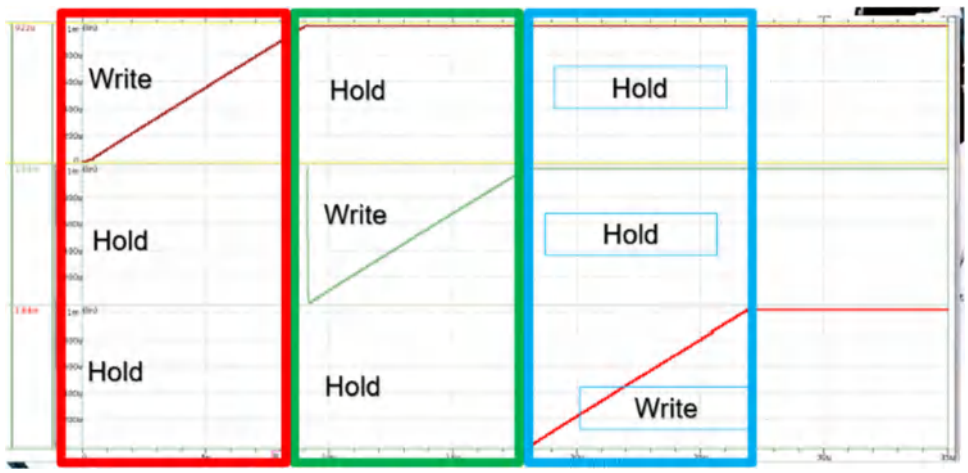



**Fig. 5** Sample and hold circuit timing diagram

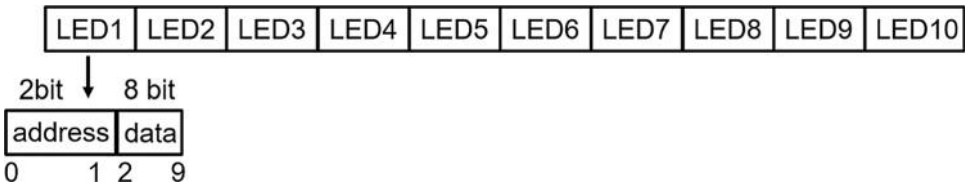



**Fig. 6** Each LED control with address and data

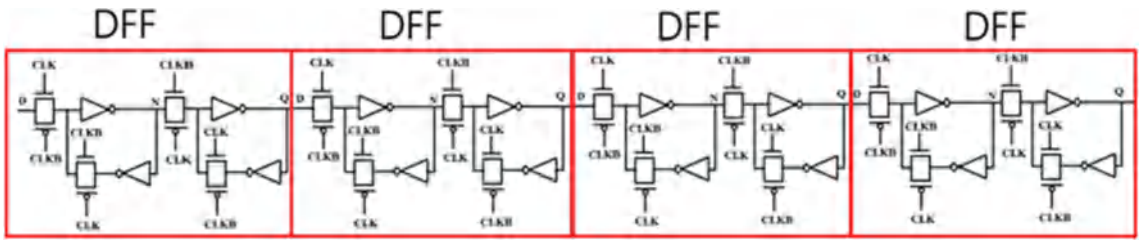



**Fig. 7** The structure of shift register

which one color component to write a new data. In this study, we design the chip to drive the 10 × 3(RGB) channel LED. Each SPI control frame is 100 bits to write the new data for one color channel, where one LED control includes 2-bit address and 8-bit data.

The SPI data transmission is one bit per cycle. The data is written to the shift register per cycle. The length of the shift register is 100 bits to store the address and data for 10 LED. In order to reduce the circuit size, we present a two-phase control shift register rather than the conventional D or JK flip-flops, where one stage only require 16 MOS (Fig. 7).

After 100 clocks, the shift register had been saved the complete data for 10 LED. The data is further latched to registers for the output. Then the other channel data can be written to the shift register again. The address 00, 01, 10 is decoded for R, G and B channel driving, respectively. The first two bits are used to decode which one color channel is active now. The first 100 bits are for red channel. The data is from the output register. The first two bits are 00, the data will be through DAC and write to the sample and hold capacitor with current mirror in Fig. 4 for 10 red LED, as shown in Fig. 8(a). After anther 100 clocks, the data for green channel had finished at the register. Similarly to red channel, the green data is written to the relative the capacitor for green LED, as shown in Fig. 8(b). At this time, the red LED current is hold for continuous light until to write a new data by scan. Finally, the blue channel is written new data when the address is 10, as shown in Fig. 8(c). The LED can be continuously light even if the scanning line is off, which can reduce the flicker. With the time sharing method, the one DAC core can drive RGB pixel. By this approach, one can save two DAC core to reduce the chip area.

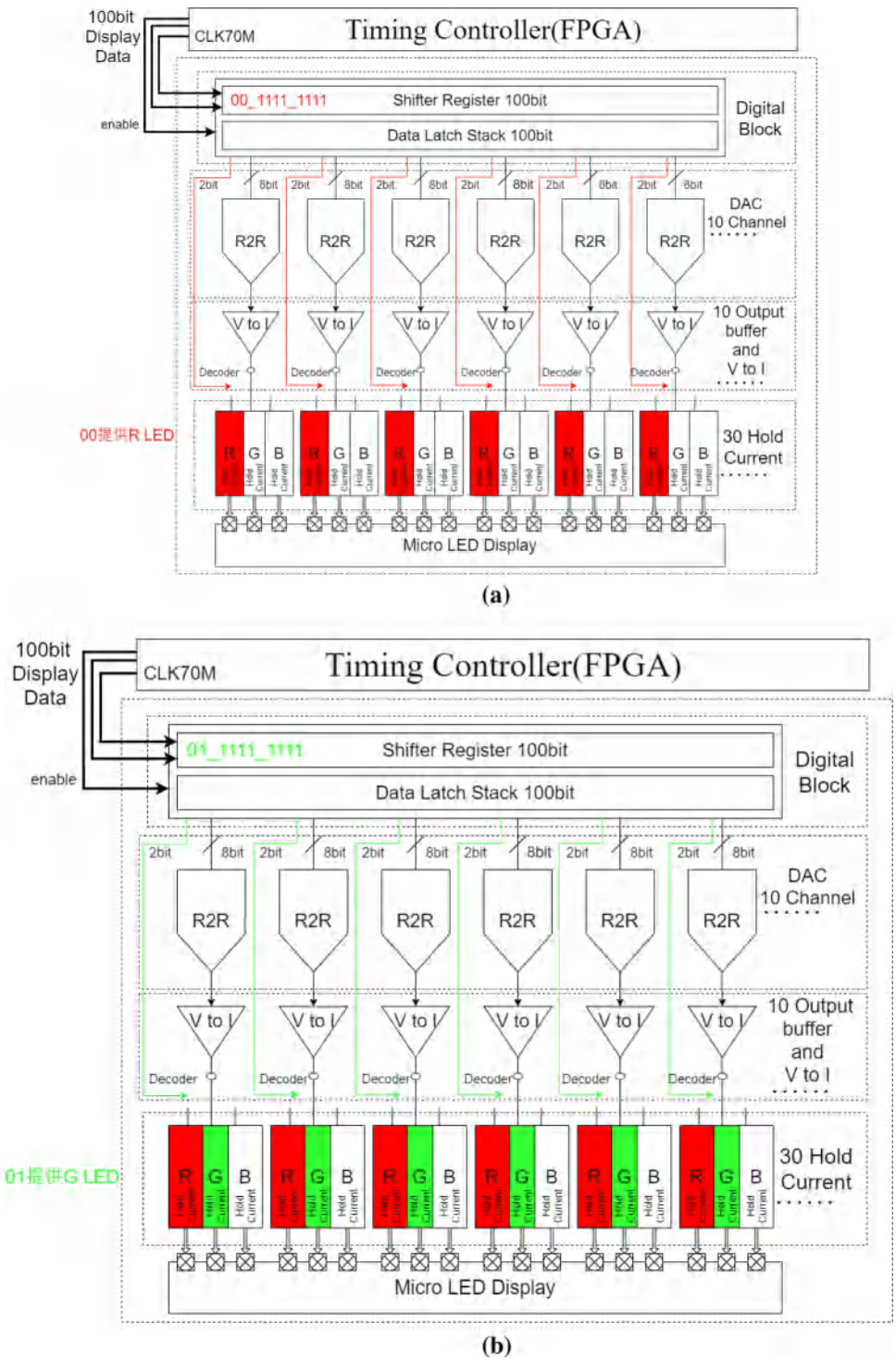



**Fig. 8** The RGB channel LED driver **a** data load for red LED, **b** data load for green LED, **a** data load for blue LED

## 3 Chip simulation and implementation

This chip is designed with TSMC 0.18UM HVG2 CMOS technology. The driver chip contains 30 channels to drive RGB LED for 10 true color pixels. The chip layout is performed with Laketool by full custom design. The layout of three channels for one color pixel, is shown in Fig. 9, where the area is 67271 um$^2$. The module contains SPI decoder, shift register, data latch, R2R-based DAC, D/I converter, RGB decoder and sample and hold circuit. The layout of the whole chip for 30 channels is shown in Fig. 10(a). The chip area is 690885 um$^2$ with 40 pins. This chip had been realized, where the micrograph is shown in Fig. 10(b).

**Fig. 8** continued

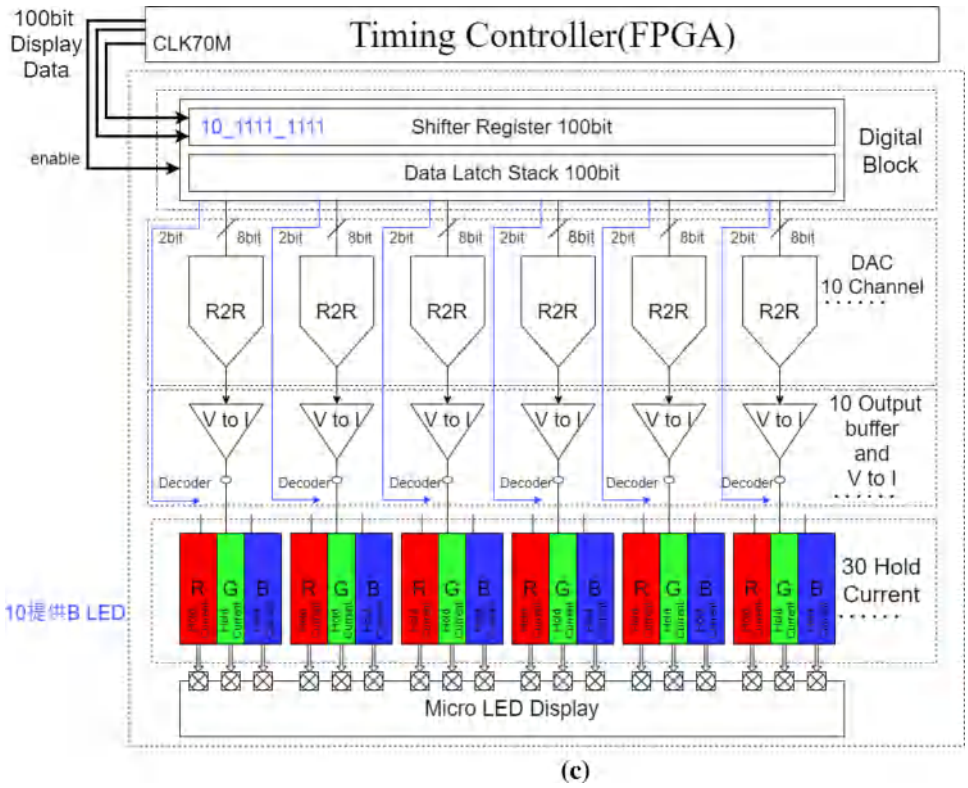
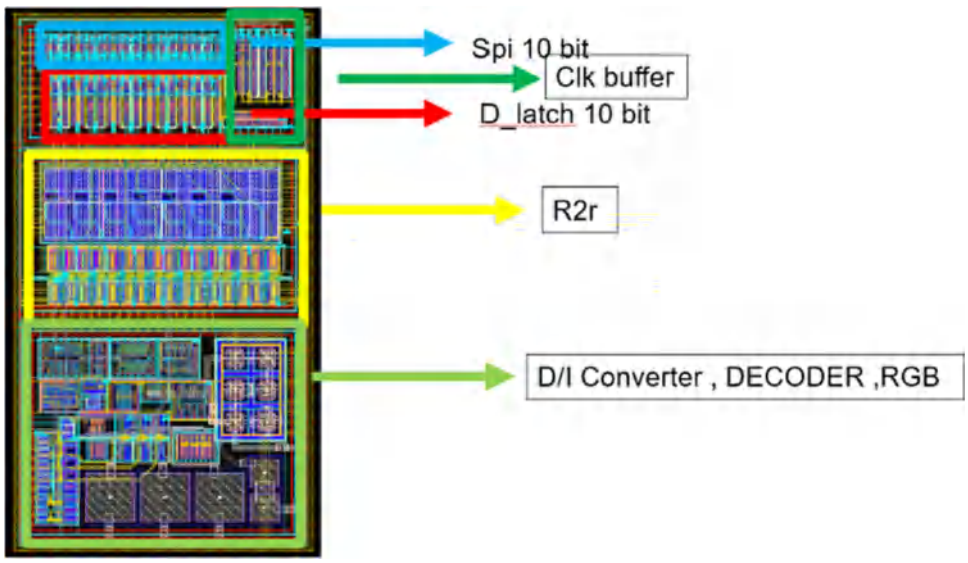
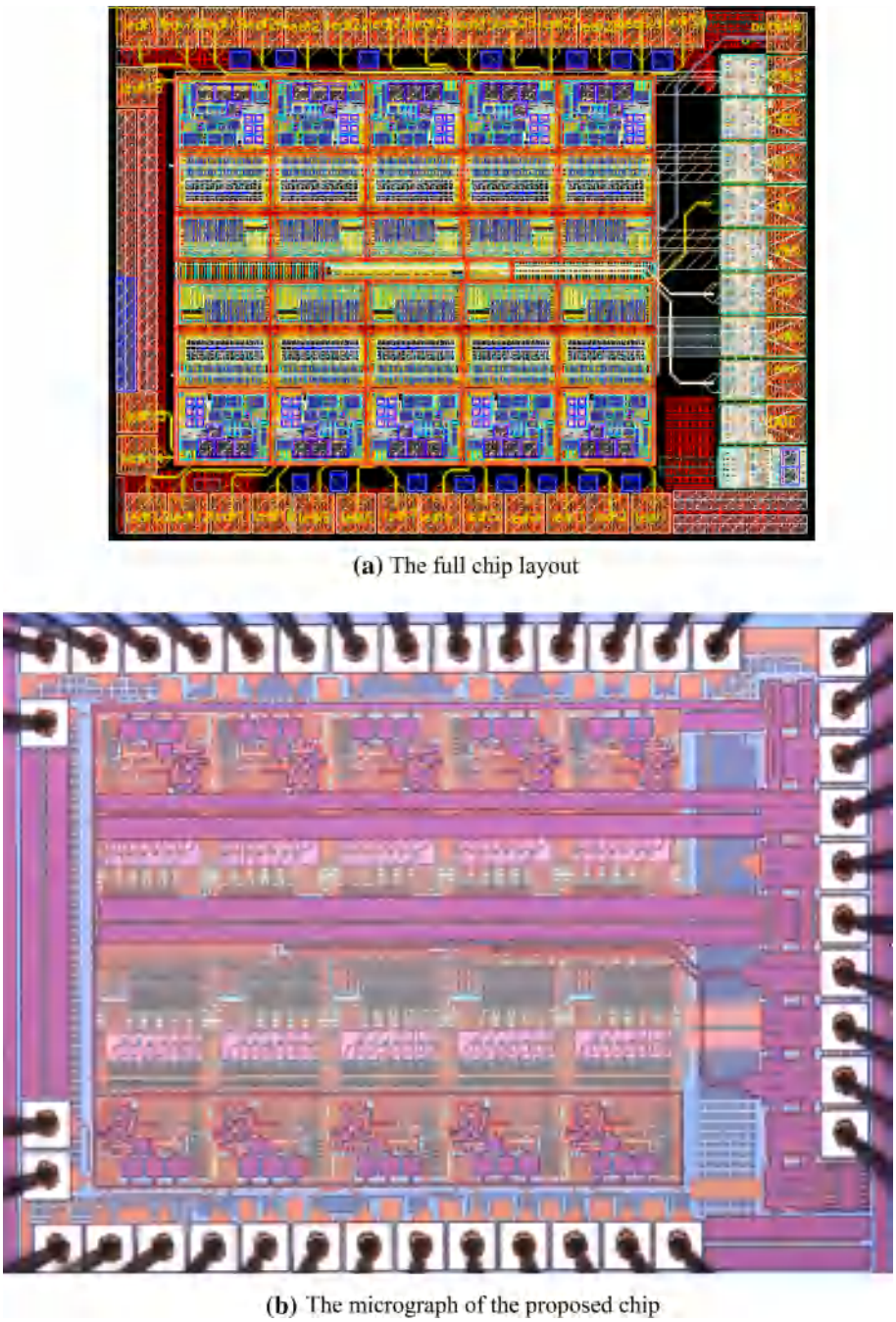



**Fig. 9** The layout of 3 channels




The resolution of each pixel is 8-bit. Each 10bit is as for the data of a channel, where the 8-bit is the dimming data, and the 2-bit is for the decoder of channel R, G, B. A row is to drive 10 color pixels, so we send 10-bit (one pixel) × 10(total pixel) = 100 bits to drive micro LED panel with three times for RGB LED. The first 100 bits are for 10 red pixels. The next 100 bits are for 10 green LED. The final 100 bits is to drive blue LED. So, the total requires 300 bits to drive 10 truth color micro LED. To simulate the function of shift register and DAC, the input data with a binary counter is from the 8-bit input digital signal 00000000 to 11111111. The data is serial input to

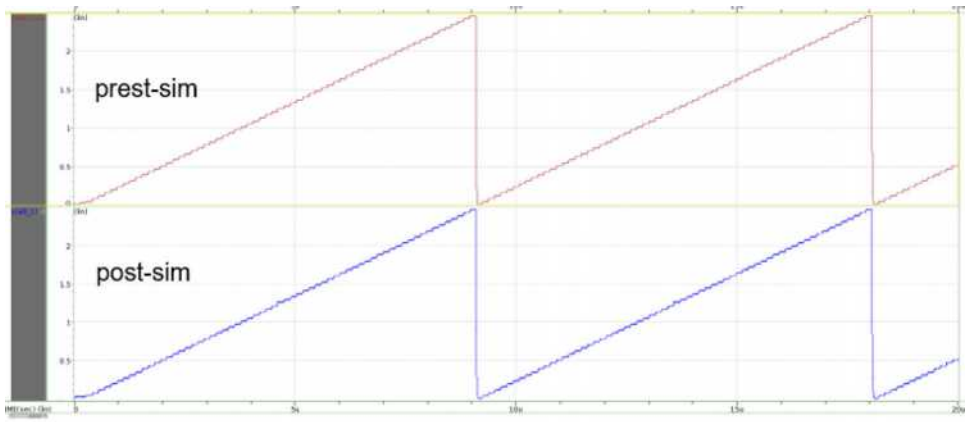


**(a)** The full chip layout

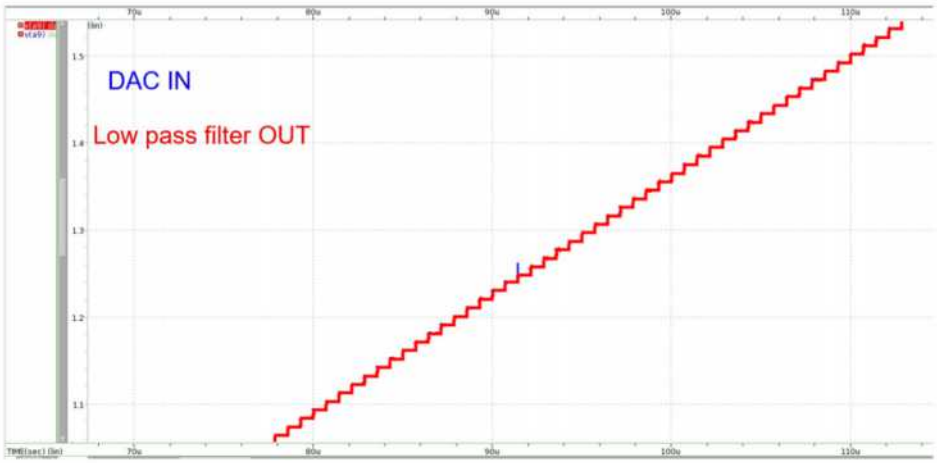
**(b)** The micrograph of the proposed chip

**Fig. 10** **a** The full chip layout. **b** The micrograph of the proposed chip

the shift register with SPI protocol. The data output in parallel to DAC. Figure 6 shows the parallel output binary counting data. Then the data input to DAC, and the results are shown in Fig. 11 for RGB LED with SAW waveform from the results of pre- and post-simulations. The binary data is high, the relative analog voltage from DAC is high too, which can keep good linear. Ti see the linear clearly, we enlarge the local region, as shown in Fig. 11(b), for the output voltage between 1.1 and 1.6 V. In order to reduce the switching noise, the low-pass capacitor is used in the output to smooth the SAW waveform.




**(a)** R2R DAC of output voltage




**(b)** Enlarge waveform between 1.1V to 1.6V output

**Fig. 11** **a** R2R DAC of output voltage. **b** Enlarge waveform between 1.1 and 1.6 V output

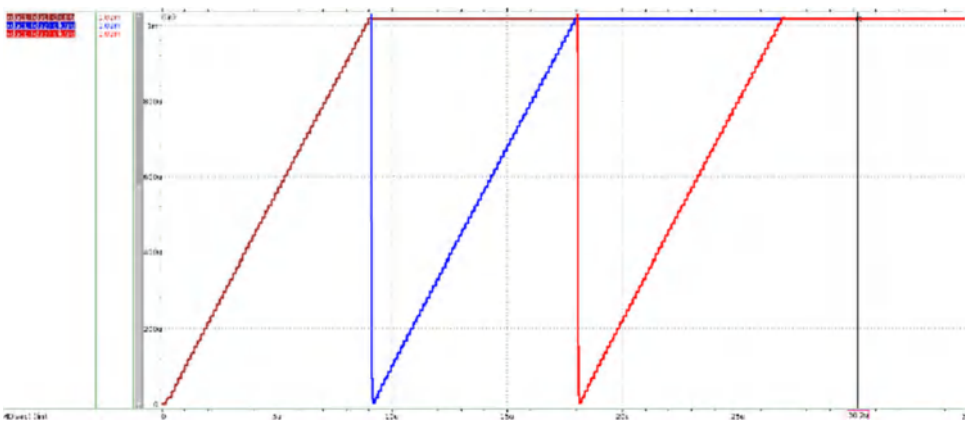


**Fig. 12** DAC voltage to current converter

Three channels share one DAC circuit. The sample and hold circuit is verified as follows. The voltage of the DAC is hold by a capacitor and converted into a current through OPA. For micro LED driving, the output voltage of the DAC is converted from 0 to 2.5 V, and converted to the current with 0–1 mA. Figure 12 shows the driving current for one pixel for RGB LED. The driving current can be

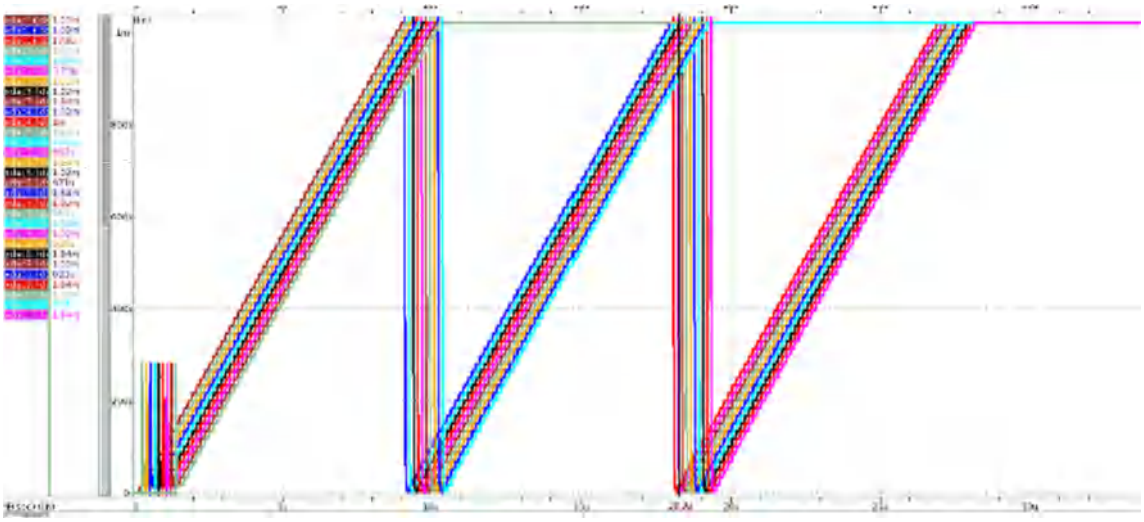
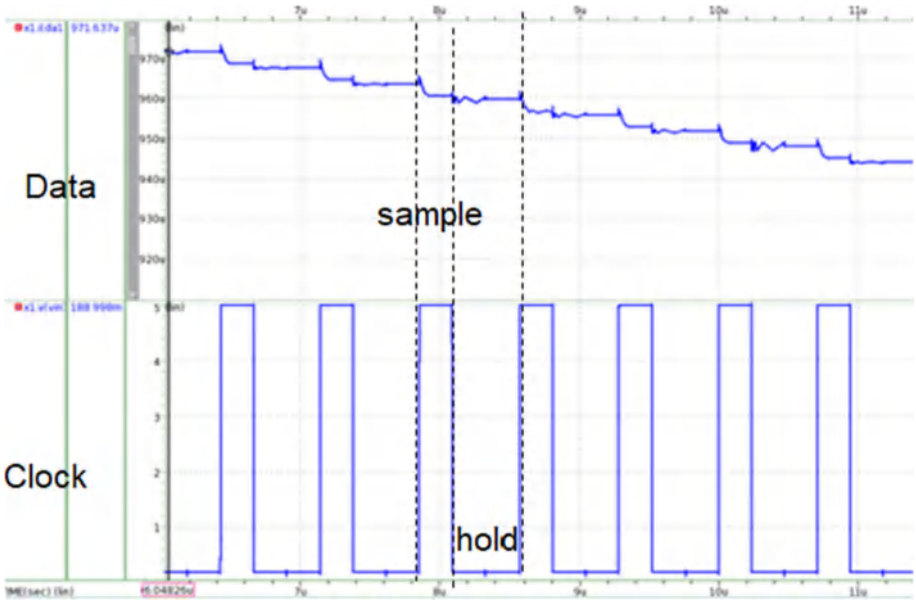


**Fig. 13.** 30 channel output current

**Fig. 14** Data sample and hold




kept when writing the other channel. One DAC can be used for 3 channels driving without current degrading.

Next, we simulate sample and hold for 10 true color pixels. First, we input 100 bit data for 10 red LED driving. The next 100 bits are for 10 green dimming, at this time, the previous 10 red LED are continuously lighting. The last 100 bits are used for blue LED. The results shows that the previous data can be hold to support the driving current without any degrading, as shown in Fig. 13 for 30 channels output current. In order to show each waveform clearly, each channel output use one delay time to show the waveform separately. Figure 14 shows the data sampling and hold for LED driving current.

## 4 Measurement and comparisons

In order to verify our proposed chip design, TSMC T18HVG2 CMOS process is used realize AM micro LED driver. FPGA chip is employed to generate the test patterns with SPI serial data and input to this chip. For the test of the driver chip, the digital signal is generated by Verilog

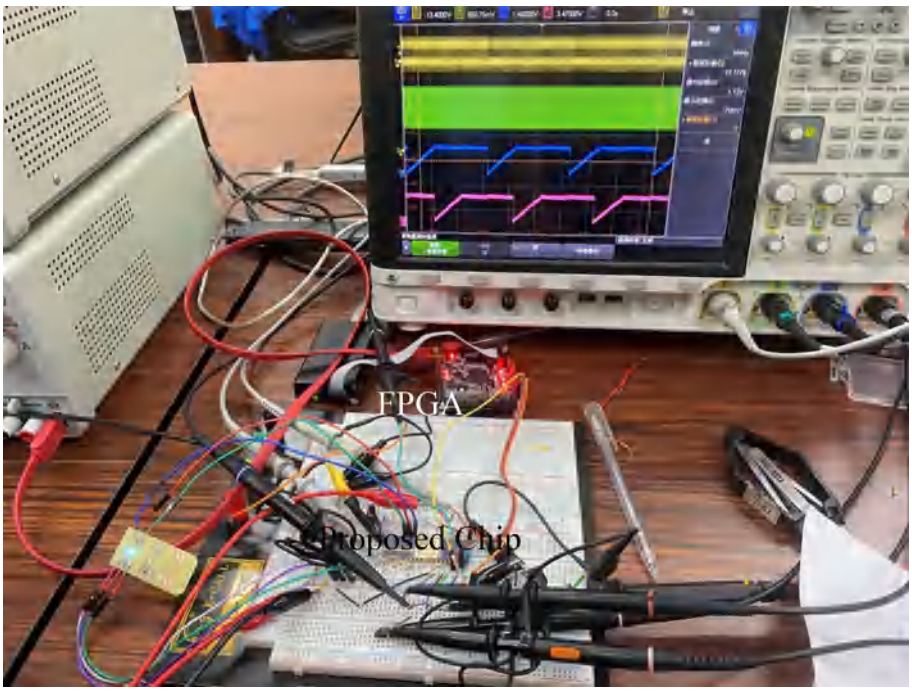



**Fig. 15** The setup of chip testing system

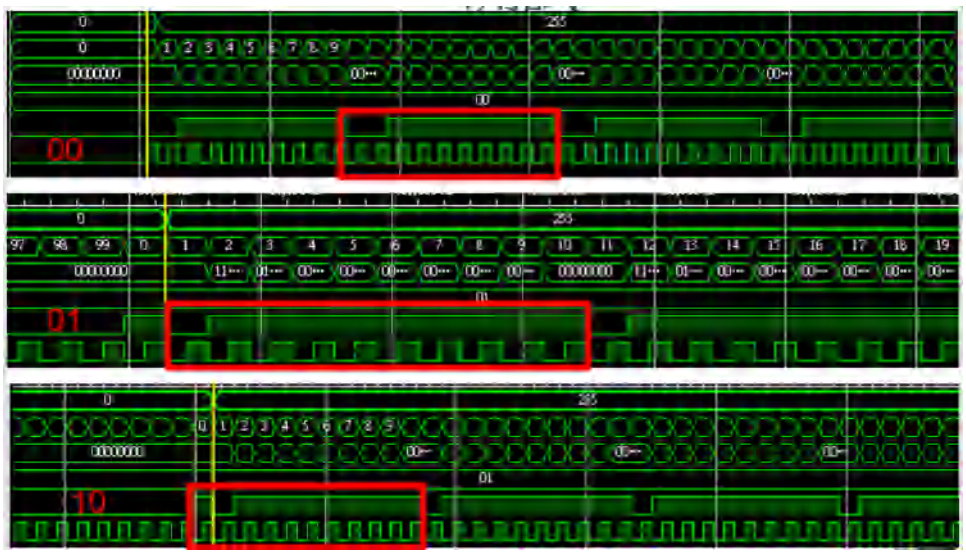



**Fig. 16** The test pattern from FPGA for RGB LED dimming respectively

code, and it compliers with Xilinix FPGA development tool. The test data is transmitted to the packaged IC through the FPGA test board, where Xinilx FPGA XC6SLX16 is employed. Figure 15 shows the setup of chip testing system. FPGA sends the relative pattern to LED dimming with SPI protocol, where the address 00,01,10 is used to control R,G, B color respectively, as shown in Fig. 16. To measure the output waveform, the output current of this chip is sensed with the current probe shown on oscilloscope. However, since the current probe cannot measure 1 mA current resolution, one use 1 k ohm as an equivalent load. The measured voltage waveform can achieve about 1 V as the maximum driving current is 1 mA. To test each case for 8-bit micro LED dimming, the input digital code from FPGA is from "0" to "255" with a binary counter. First, we sent 100 bits for blue micro LED channel with 256 times. The first sent 255 code to 10 channels, each channel is 10 bits. The second, third sent 354,253 to this test chip. Following this procedure, at the final step, the zero code feeds to this chip. Results show that the output waveform is a linear ramp from high to low. The results are shown in Fig. 17. As the blue channel is completely sent, the next data is for the red channel micro LED. Similarly to the blue channel, we sent $100 \times 256$ bit to measure the waveform of red channel. The

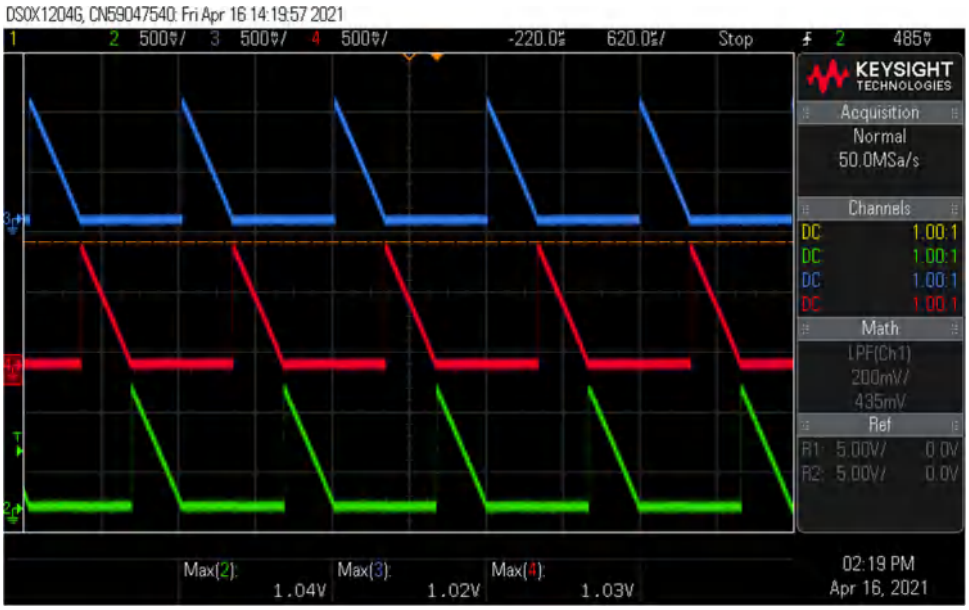



**Fig. 17** 3 channel output current

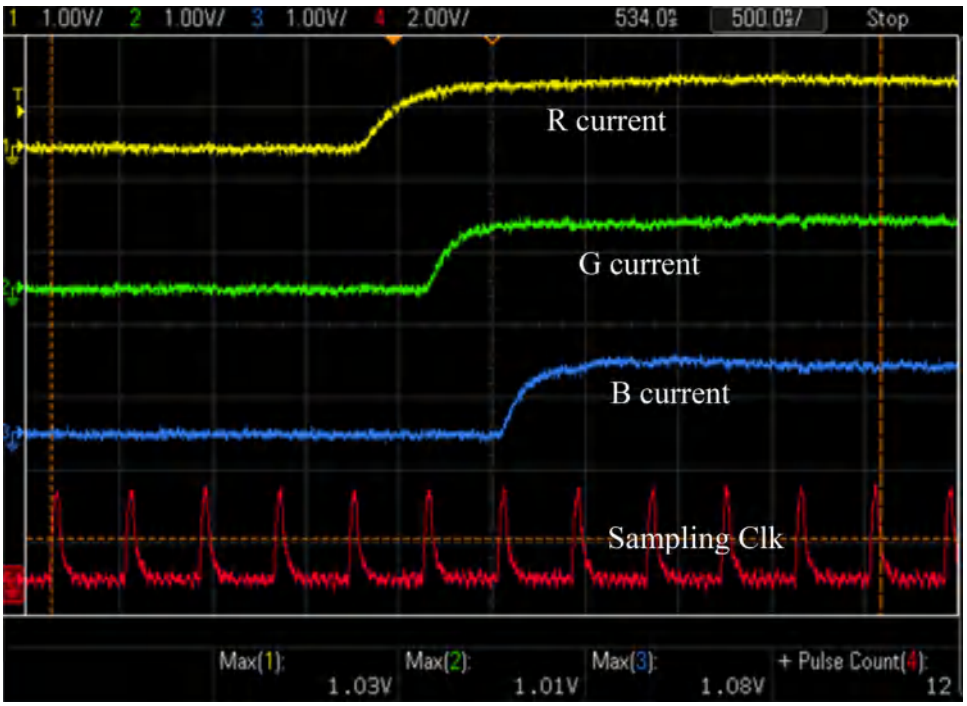



**Fig. 18** The data holding for RGB LED

result shows that the ramp waveform of red channel outputs at end of blue channel. The finally channel is measured for the green micro LED. Since this chip implements 30 channels, it can drive 10 pixels per 100 clocks. When 10 RGB pixel are completely done, the next 10 color pixel of micro LED is following to display with SPI decoder. With the active matrix driving, the previous pixel value can be hold to avoid flicker problem.

Figure 18 shows the output current for R,G,B channel with the sampling and hold. At the first sampling clock, R data is sent and the data is hold at the C1 capacitor. The voltage is maintained until to the next scanning data input to refresh the data. Similarly, R and B current is hold with the capacitor C2 and C3 respectively. Next, we measured the output response time of the channel output. To consider the worst case, the output current is tested from the zero current to the maximum current from this driver IC, where the input digital code is from "0" rising to "255". The rise Time is 273.5 ns. The falling time is about 0.24us. The result is shown in Fig. 19(a, b) for the rising time and

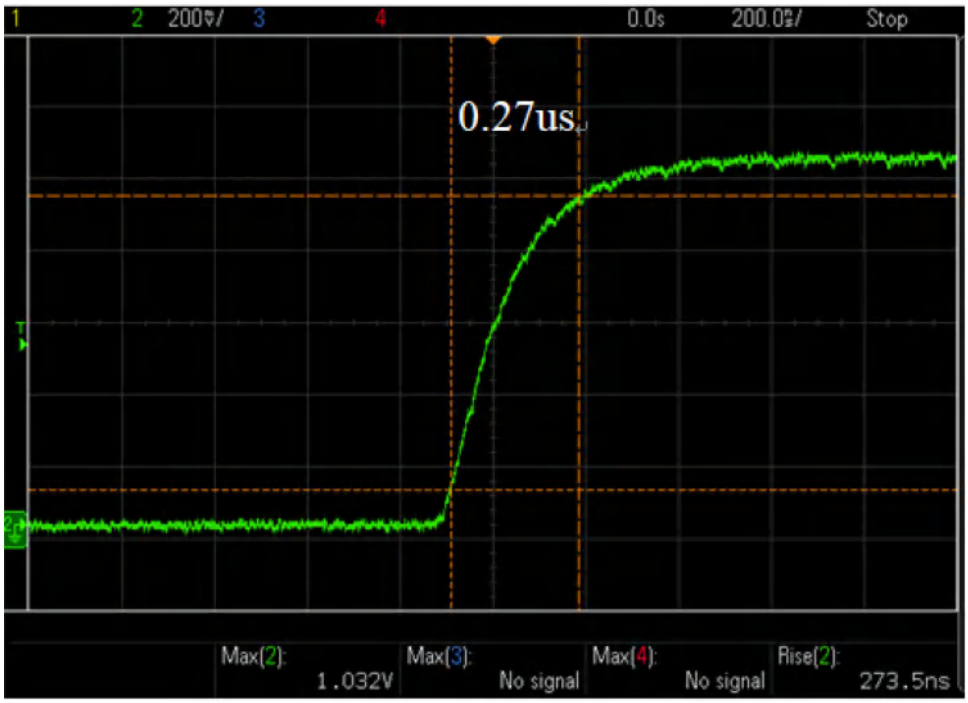



**Fig. 19** The rising time measurement from the zero current to the maximum current **a** rising time, **b** falling time

falling time respectively. In the worst case, the refresh time is about 0.6 us.

Next, we measure the linear feature between the output current and input data. Figure 20(a) shows the DNL value, where the error is about + 0.201/− 0.0013. The error of INL is + 0.02/− 0.204, as shown in Fig. 20(b). Table 1 lists the features of our chip. This chip is designed to drive 30 micro LED for 10 true-color pixel with 8-bit resolution. The chip area including I/O pads is about only 1.3 $mm^2$, where used only about 5 k transistors. The maximum driving current is 3 mA. The linear of DAC is excellent, where DNL and INL is about 0.3–0.4 LSB, with a mathlab

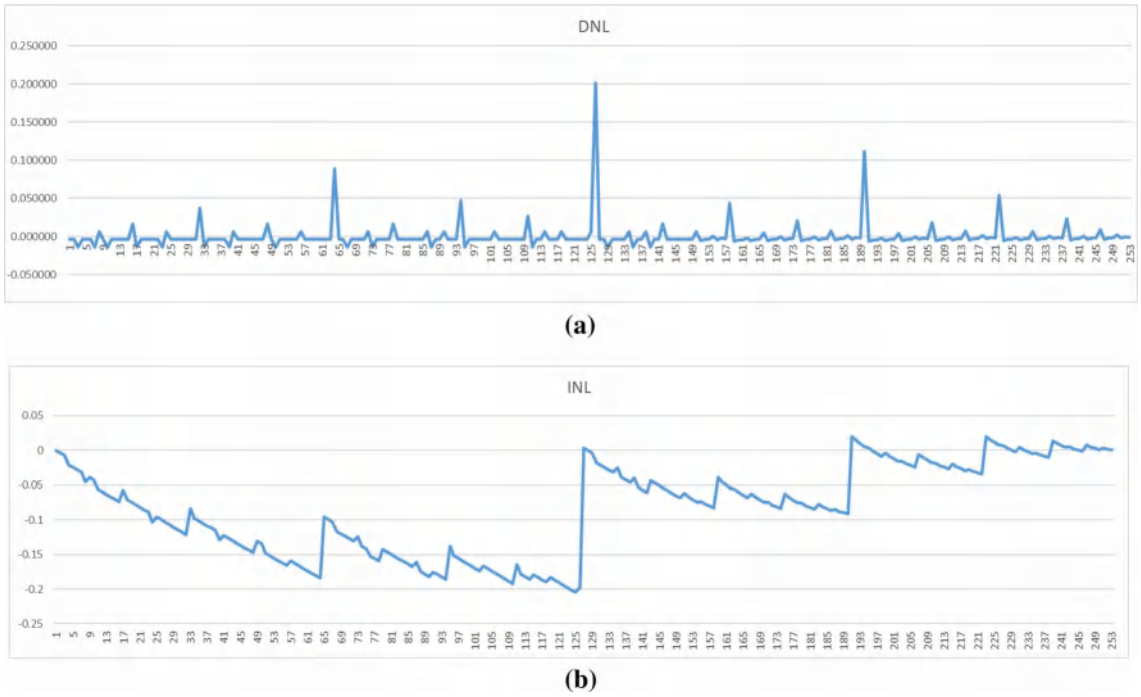



**Fig. 20** Measurement of linear feature. **a** The DNL value, **b** INL value

**Table 1** Chip features

| 70Meg 10*3 channel DAC | |
|---|---|
| Technology | T18HVG2 |
| Channel | 10 * 3 |
| DNL | + 0.201/− 0.013 |
| INL | + 0.02/− 0.204 |
| One channel area (um$^2$) | 67,271 |
| Whole chip area (mm$^2$) | 1.308 |
| Max. out current | 3 mA |
| Mosfets | 4674 |
| Elements | 4957 |
| Power supply | 5 V |
| Resolution/bit | 8 |
| Passive/active | Active |
| Frame bit | 100 |
| Clk frequency | 70Meg |
| DAC architecture | R − 2R |
| Number of LED\PIXEL | 30\10 |

tool. The number of MOS used 4657. The maximum working frequency is 70 MHz for the digital circuit. So the refreshing one row requires 14.3 ns × 300 = 4.29 us, which is enough fast for real-time display.

Table 2 lists the comparisons with the existed AM driving chips. Lu et al. [5] presented a 10-bit two-Stage R-DAC with isolating source followers, which DAC is designed with 6-bit positive signal combined with 6-bit negative signal. An et al. [9] presented a 24-channel time-shared 8-bit digital-to-analog converter (DAC) with dual sampling to minimize the effective channel area of the column driver. Kim et al. [11] design a source-driver IC that actively compensates for inter-channel charging rate mismatch in an active-matrix, where a digital method controls gm-degeneration technique. Bang et al. [21] proposed a bit-inversion cascade to realize the DAC without using resistors, which employed 44 MOS rather than divided resistors.

In this study, we present R2R DAC to realize the current drive for the micro LED display. The number of resistors and switches of DAC unit is only 18 and 8, which can be greatly reduced compared with the existed driver with R DAC or like R DAC method. Besides, this method does not

**Table 2** Comparisons with AM Micro-LED driving chips

| | Bang16' [21] | Kim' 18 [11] | An18' [9] | Lu'19 [5] | Proposed |
|---|---|---|---|---|---|
| Process | 0.18um | 0.18um | 0.13um | 0.18um | 0.18um |
| DAC type | Bit-inversion cascade | R DAC | 6-bit RDAC + 2-bit Amp | 6-bit Positive + 6-bit Negative | R/2R |
| No. of resistor in DAC | 44 | 256 | 64 | 160 | 18 |
| No. of switch in DAC | 16 | 255 | 65-to-2 Mux | 128 | 8 |
| Gray level | 8 bits | 8 bits | 8 bits | 10 bits | 8 bits |
| DNL/IDL | 0.75/0.56 LSB | 0.4/0.52LSB | 0.07/0.24 LSB | 0.6/0.77 LSB | 0.31/0.35 LSB |
| Max. output Voltage | 5 V | 4.3 V | 5 V | 4.75 V | 4.85 V |
| DC current | 10cuA | 1.4 uA | 3.02 uA | 1.5 uA | 0.32 uA |
| No. of channel | 102 | 240 | 24 | 24 | 30 |
| Area reduction | – | – | – | 43% | 66% |

require the decoder circuit, which can reduce the decoding time. With time-sharing method, RGB channels are driven with the common DAC core, which can save 66% silicon area. For micro LED application, the maximum driving current is designed with 1 mA that is enough to drive *u*LED, and the current resolution achieves about 4 uA for gray level control with 8-bit dimming.

The main difference of this driver from other publications is follows. (1) This chip used the R2R circuit rather than R DAC structure. The number of switches and resistors can be greatly reduced while keeping excellent linearity. (2) The selected current mirror structure in Fig. 4 is proposed with time-sharing method. This approach can save 2/3 DAC cores and to reduce the power dissipation as well. (3) The complete digital core is designed with serial data input and output data to the micro LED in real-time processing. The maximum frequency can achieve 70 MHz with SPI interface for real-time display. (4) The chip with mixing-mode layout is very dense, which includes the analog and digital circuit. The chip can drive 30 channels micro LED with only 67,271 $um^2$ silicon area. The prototype is successfully measured, and the results show with high performance and good quality in experiments. The chip module can be expanded for large panel with cascade method through SPI interface.

## 5 Conclusions

In this paper, we proposed three-channel with the common driver to save the circuit complexity, which could be applied for Micro LED displays. In order to enable the panel to achieve active matrix displaying, the signal is decoded for each channel and through the sampling and hold circuit to keep the previous dimming data based on the selected current mirror control. Combined with FPGA testing, the results shows the data can be kept during off-scanning period, which can reduce flicker for micro LED displaying. The proposed 30 channel constant current micro LED driver had been realized with a small silicon area, which the digital frequency can operate up to 70 MHz. The refresh time for one row is only about 5 us. Experimental results show that this chip for micro LED driver is successful implementation for 8-bit gray current with good linear and low power.

**Data availability** Raw data were generated at the VLSI lab. in Department of Electronics Engineering, National Yunlin University of Science and Technology.

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